

## CLAIMS

What is claimed is:

1. A method for designing a rerouting element for use with a semiconductor device including at least one bond pad positioned substantially centrally on a surface thereof, comprising:  
configuring at least one contact location on a first surface of a substantially planar member, said at least one contact location mirroring a position of the at least one bond pad on the surface of the semiconductor device;  
configuring at least one conductive trace location extending from said at least one contact location toward a periphery of said substantially planar member; and  
configuring at least one rerouted bond pad location proximate said periphery, said at least one rerouted bond pad location being configured to be exposed beyond a periphery of another semiconductor device upon positioning said another semiconductor device over the surface of the semiconductor device.
2. The method of claim 1, wherein said configuring at least one contact location comprises configuring a plurality of contact locations, each contact location of said plurality of contact locations mirroring a location of a corresponding bond pad on the surface of the semiconductor device.
3. The method of claim 2, wherein said configuring at least one conductive trace location comprises configuring a plurality of conductive trace locations, each conductive trace location of said plurality of conductive trace locations extending from a corresponding contact location toward said periphery of said substantially planar member.
4. The method of claim 3, wherein each conductive trace location of said plurality of conductive trace locations extends toward a single edge of said substantially planar member.

5. The method of claim 3, wherein said configuring at least one rerouted bond pad location comprises configuring a plurality of rerouted bond pad locations, each rerouted bond pad location of said plurality of rerouted bond pad locations being continuous with an end of a corresponding conductive trace location and located proximate said periphery of said substantially planar member.

6. The method of claim 5, wherein each rerouted bond pad location of said plurality of rerouted bond pad locations is configured to be exposed beyond a periphery of said another semiconductor device upon positioning of said another semiconductor device over the surface of the semiconductor device.

7. The method of claim 1, wherein said configuring said at least one rerouted bond pad location comprises configuring said at least one rerouted bond pad location to facilitate connection of a discrete conductive element thereto with said another semiconductor device positioned over the surface of the semiconductor device.

8. A method for assembling semiconductor devices in a stacked arrangement, comprising:  
providing a semiconductor device with at least one bond pad positioned substantially centrally on a surface thereof; and  
positioning a rerouting element over said surface of said semiconductor device with a contact of said rerouting element communicating with said at least one bond pad, a circuit trace of said rerouting element extending laterally toward a periphery of said semiconductor device and establishing communication between said at least one bond pad and at least one rerouted bond pad located proximate a periphery of said semiconductor device at a location where said at least one rerouted bond pad will remain exposed upon positioning another semiconductor device over said surface.

9. The method of claim 8, wherein said providing said semiconductor device comprises providing a semiconductor device with a plurality of bond pads, at least some of which are positioned at substantially central locations on said surface.

10. The method of claim 9, wherein said positioning said rerouting element comprises positioning a rerouting element comprising:  
a plurality of contacts, each contact of said plurality of contacts being positioned correspondingly to a position of a corresponding bond pad of said semiconductor device;  
a plurality of conductive traces, each conductive trace of said plurality of conductive traces extending laterally from a corresponding contact of said plurality of contacts toward said periphery of said semiconductor device; and  
a plurality of rerouted bond pads, each rerouted bond pad of said plurality of rerouted bond pads being positioned at an end of a corresponding conductive trace, proximate said periphery of said semiconductor device.

11. The method of claim 10, wherein said positioning said rerouting element comprises positioning a rerouting element with each rerouted bond pad of said plurality of rerouted bond pads being positioned proximate a single peripheral edge of said semiconductor device.

12. The method of claim 10, wherein said positioning said rerouting element comprises positioning a rerouting element with each rerouted bond pad of said plurality of rerouted bond pads being positioned to be exposed beyond a periphery of another semiconductor device upon being positioned over said surface of said semiconductor device.

13. The method of claim 8, further comprising:  
positioning another semiconductor device over said rerouting element, said at least one rerouted bond pad of said rerouting element being exposed beyond a periphery of said another semiconductor device.

14. The method of claim 13, further comprising:  
securing said semiconductor device to a carrier substrate.

15. The method of claim 14, wherein said securing comprises securing said semiconductor device to at least one of a circuit board, an interposer, an additional semiconductor device, and leads.

16. The method of claim 14, further comprising:  
positioning at least one discrete conductive element between said at least one rerouted bond pad and a corresponding contact area of said carrier substrate.

17. The method of claim 16, wherein said positioning comprises at least one of wire bonding, tape-automated bonding, and thermocompression bonding.

18. The method of claim 14, further comprising:  
encapsulating at least portions of said semiconductor device, said another semiconductor device, and regions of said carrier substrate adjacent to said semiconductor device.

19. The method of claim 18, wherein said encapsulating comprises glob top encapsulating.

20. The method of claim 18, wherein said encapsulating comprises one of transfer molding and pot molding.